

Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

Replacement drawing sheets contain printed reference numerals.

The new Abstract better describes the disclosure.

The amended independent and depending claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

Independent claim 21 defines circuitry comprising plural data output paths, a control signal input path, and a scan path.

The each of the plural data output paths include a tri-state output buffer having a data input, a data output and a control input.

The control signal input path includes an input buffer having a signal input and a signal output.

The scan path exists between a test data input lead and a test data output lead.

The scan path includes a first scan cell having a functional data input connected to the signal output of the input buffer. The functional data output is connected to the control inputs of all the output buffers. A test data input is coupled to the test data input lead. A test data output is separate from the functional data output.

The scan path includes second scan cells. Each second scan cell has a functional data input, a test data input, and a combined data output of functional data and test data.

The second scan cells are connected in a series with the test data input of the initial second scan cell in the series being connected to the test data output of the first scan cell. The combined data output of each second scan cell is connected to the test data input of the next, successive second scan cell. The combined data output of each second scan cell is also directly connected to the data input of one tri-state output buffer.

The scan path includes multiplexer circuitry having one input connected to the combined data output of the last second scan cell in the series, another input connected to the test data output of the first scan cell, and an output coupled to the test data output lead.

In contrast, US 5,701,308 to Attaway depicts in Figure 3A a scan cell suitable for use as a boundary scan test cell, which in Figure 4 is included in boundary scan register 20. The scan cell of Figure 3A has a functional or normal data output NDO separate from a test or serial data output SDO.

Figure 3B depicts a scan cell for performing a scan test of internal circuitry, which in Figure 4 is included in internal scan register 18. The scan cell of Figure 3B has a combined data output of functional or normal data NDO and test or serial data SDO.

Figure 4 depicts a connection of the output of internal scan register 18 and the output of boundary scan register 20 as inputs to multiplexer 32. The output of internal register 18, which scan cells have combined data outputs of

functional and test data, can selectively be coupled to the input of the boundary scan register 20, which scan cells have separate functional and test data outputs.

Present independent claim 21 requires plural data output paths with each path including a tri-state output buffer having a data input and a control input. A control signal input path includes an input buffer having a signal output. A scan path of scan cells and a multiplexer exists between a test data input lead and a test data output lead.

Claim 21 requires a first scan cell having a functional data input connected to the signal output of the input buffer, a functional data output connected to the control inputs of all the output buffers, a test data input coupled to the test data input lead, and a test data output separate from the functional data output.

Claim 21 requires second scan cells connected in a series. Each second scan cell has a test data input, and a combined data output of functional data and test data. The test data input of the initial second scan cell in the series is connected to the test data output of the first scan cell. The combined data output of each second scan cell is connected to the test data input of the next, successive second scan cell. The combined data output of each second scan cell also is directly connected to the data input of one tri-state output buffer.

Claim 21 requires multiplexer circuitry having one input connected to the combined data output of the last second scan cell in the series, another input connected to the test data output of the first scan cell, and an output coupled to the test data output lead.

These specific limitations distinguish over the disclosure in the Attaway patent.

US 6,343,365 to Matsuzawa discloses in Figure 2A the selective connection of internal scan path 11 and I/O (boundary) scan path 10, in Figure 2B the selective connection of internal scan path 11, I/O (boundary) scan path 10, and internal scan path 11, and in Figure 2C the selective connection of I/O (boundary) scan path 10, internal scan path 11, and I/O (boundary) scan path 10.

The specific limitations of independent claim 21 distinguish over the disclosure in the Matsuzawa patent.

The combined disclosure of the Attaway and Matsuzawa patents fail to disclose or suggest the specific limitations, reiterated above, of independent claim 21.

Claim 21 stands allowable.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

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